I. PROTOCOLS DESCRIPTION

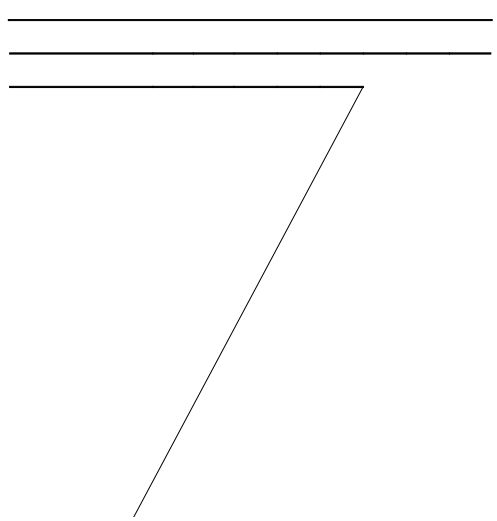
I.2 PIF Protocol

I.2.1 Overview

The PIF protoco

Single-data read request
Single-data write request
Block-read request (equivalent to the incremental-burst read transfer in WISHBONE protocol)
Block-write request (equivalent to the incremental-burst write transfer in WISHBONE protocol)
Read-conditional-write request

The bridge, as it will be explained in the following chapters, does not support the read-conditional-write transfer because this type is not present in the WISHBONE standard.
To perform the request and specify the type of transfer, the PIF protocol uses the ReqCNTL signal; below it's explained the meaning of the different bits:



II.1 OVERVIEW

Figure 1 below shows general architecture of PIF / WISHBONE BRIDGE core. It consists of two main building blocks:

PIF to WISHBONE Bridge: it has a SLF

transfers betwt

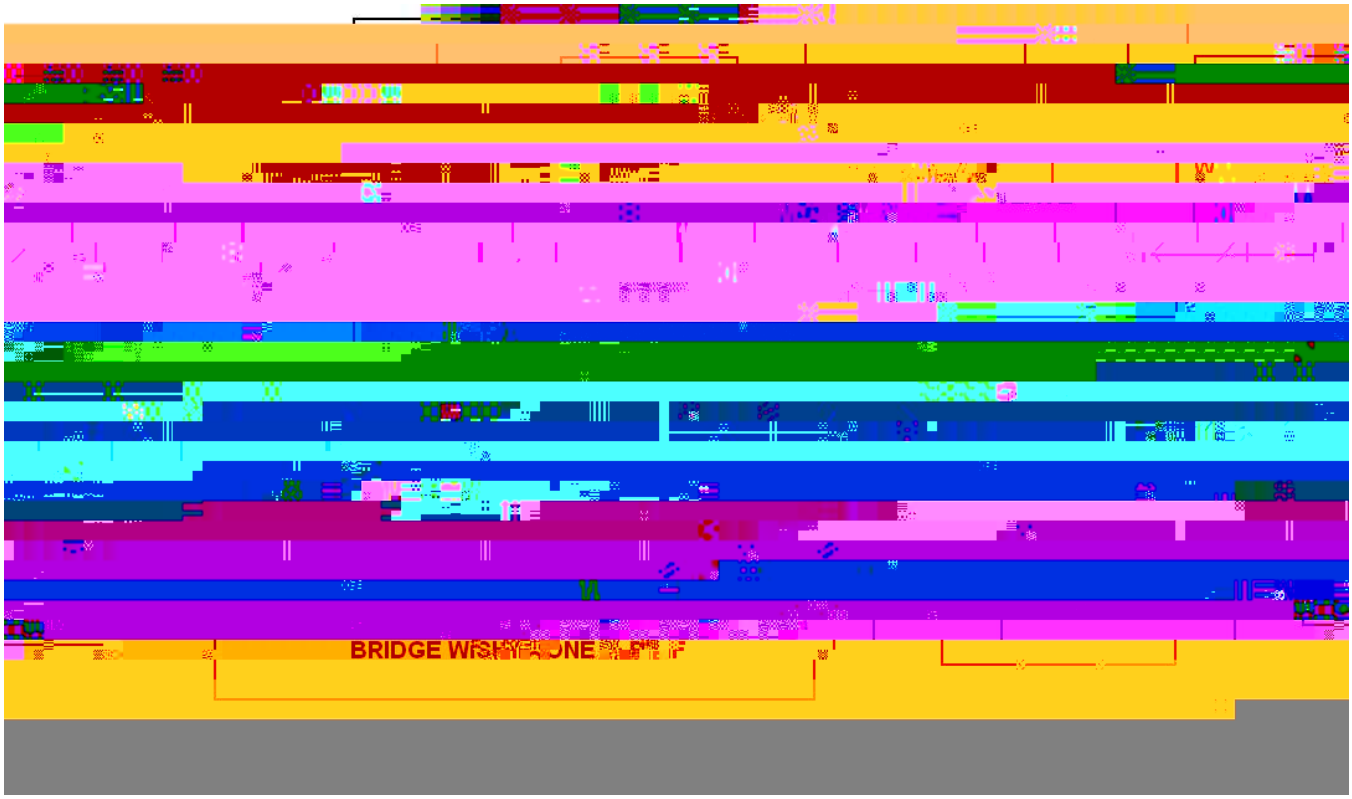


Figure 2 ± Bridge PIF / WISHBONE Architecture

II.2 THE I / O PORTS

The signals used by the two protocols and described in chapter I represent the input and output ports of the bridge, because it must be able to connect

Note

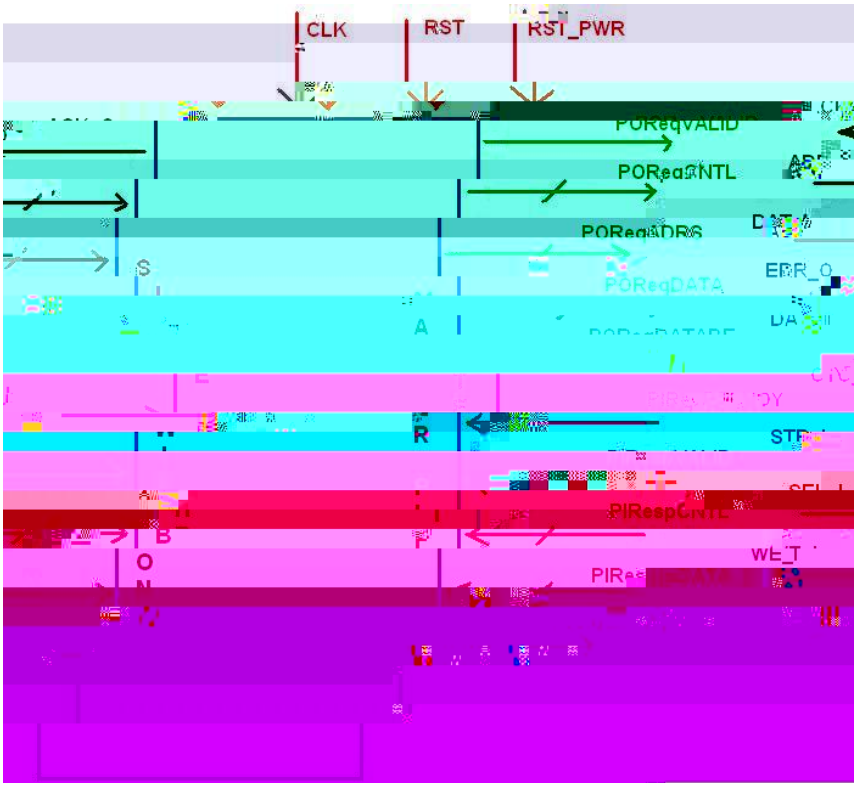


Figure 4 ± WISHBONE to PIF

Vr ngth: B@@r

About the I/O signals, the two protocols allow to have signals with different length: for example the data size can have some fixed values and the same is for the address. So, to make the bridge more compliant with different IP#gw VVe codes, at the beginning of each VHDL source file are dae ss ars kSg vl O#o

2. the most cycle types are provided by both the protocols; these t

specified by the master at beginning of the cycle and it can assume any value.

3. The error codification code m

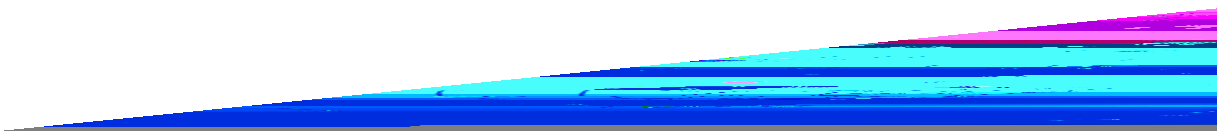


Figure 7 ± WISHBONE to PIF FSM

To realize the design of the two FSM, I studied the two protocols to

III. DIAGRAMS

III.1 WISHBONE to PIF ± Single Write Cycle

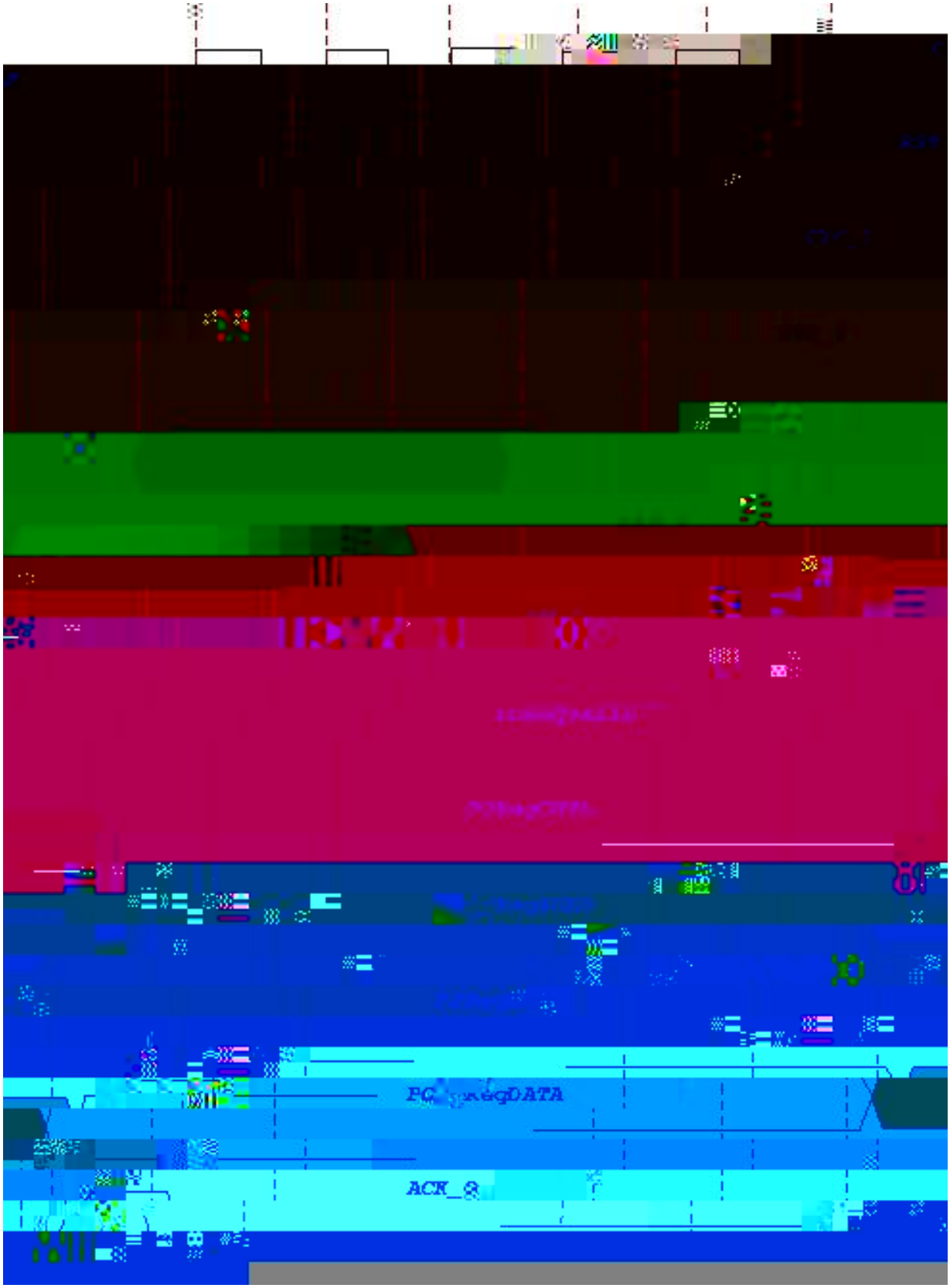


Figure 8 ± WISHBONE to PIF single write cycle

III.4 PIF to WISHBONE ± B&À

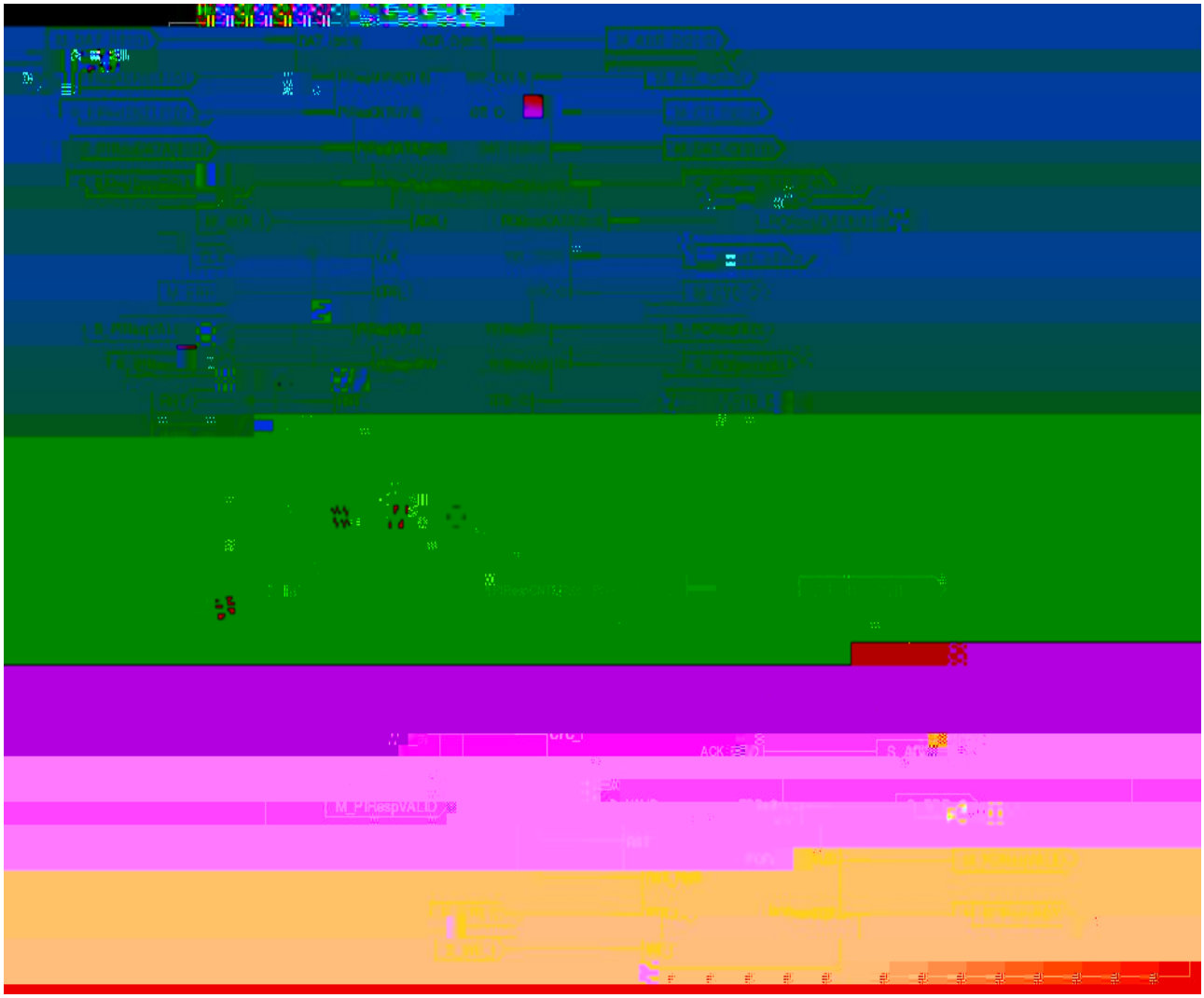


Figure 12 ± Bridge RTL schematic

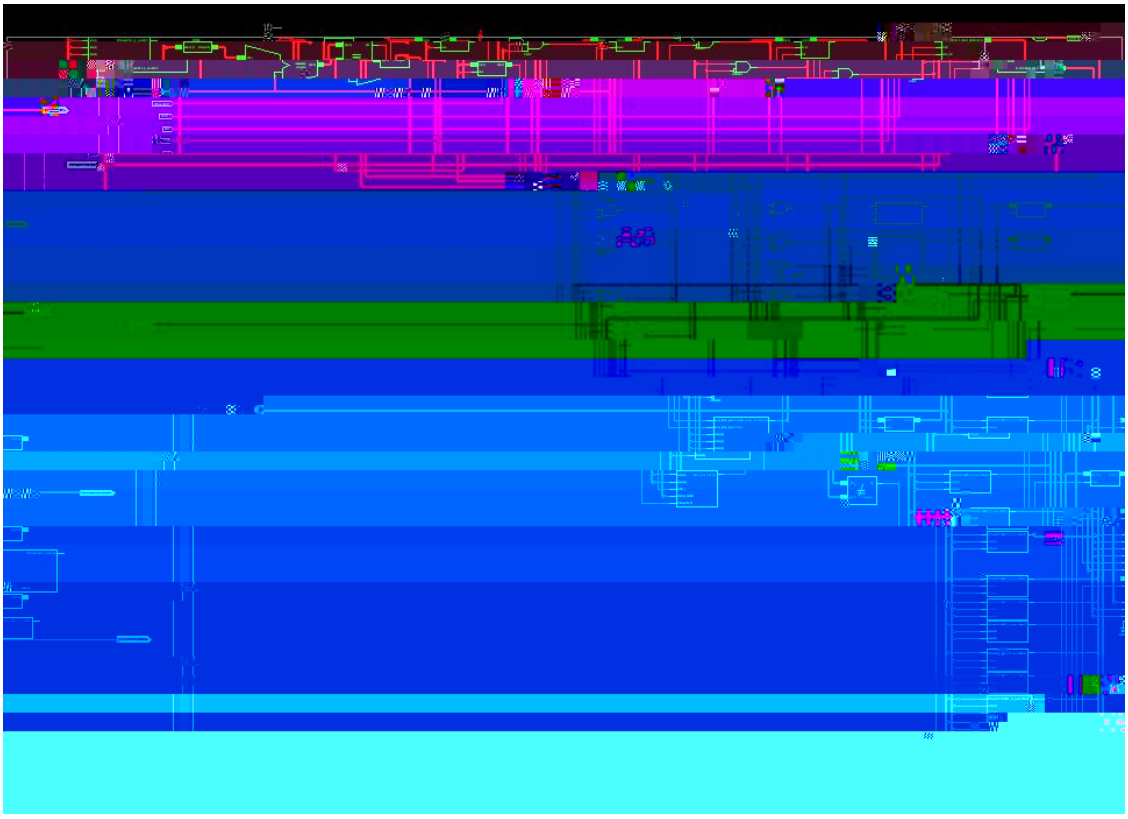


Figure 13 ± PIF to WISHBONE RTL schematic

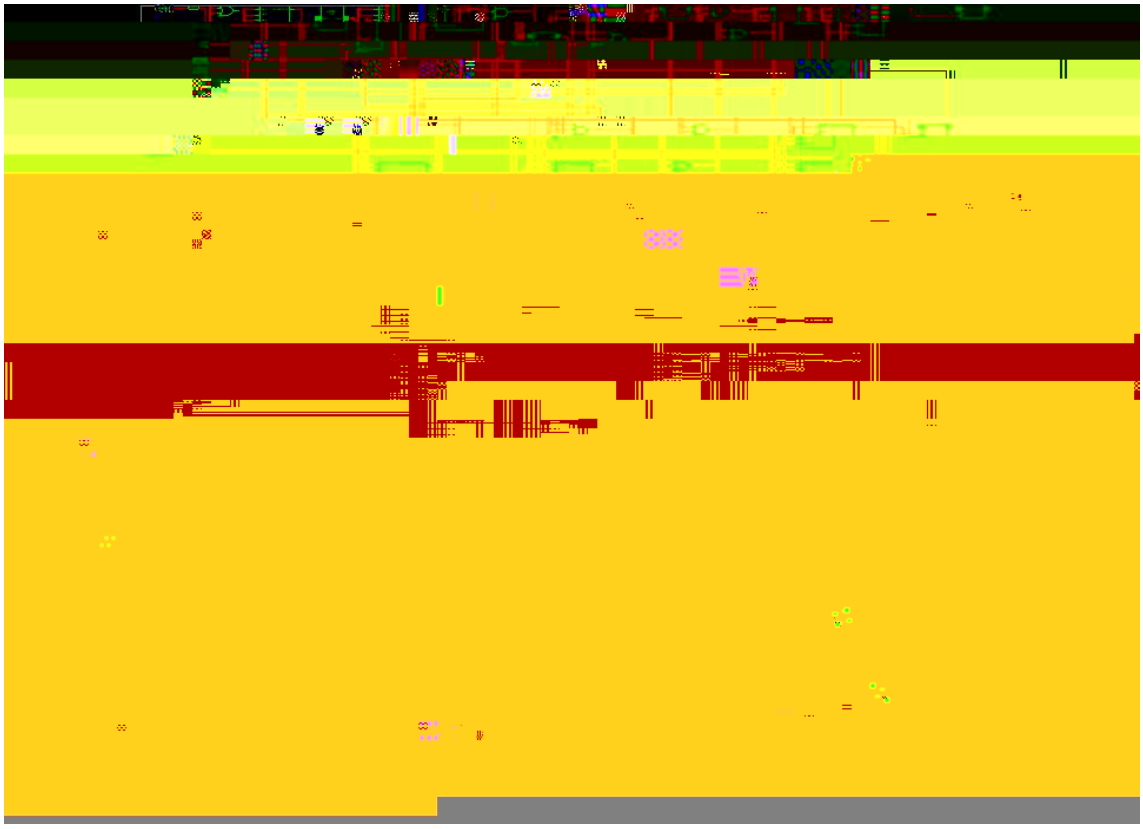
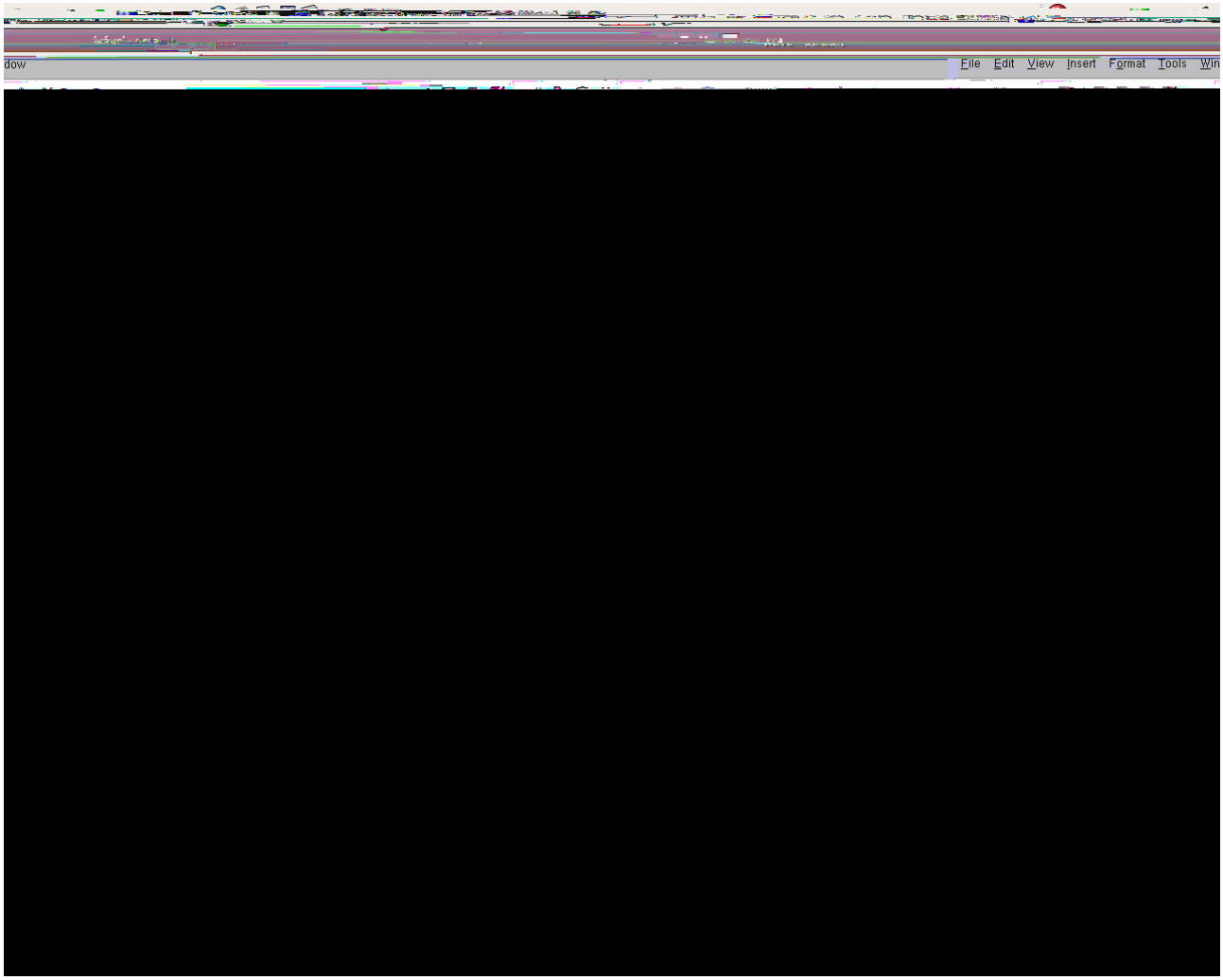


Figure 14 ± WISHBONE to PIF RTL schematic

Below you find the design summar

Figure 15 ± Compile Flags for Block read / write


dow
File Edit View Insert Format Tools Win

Figu

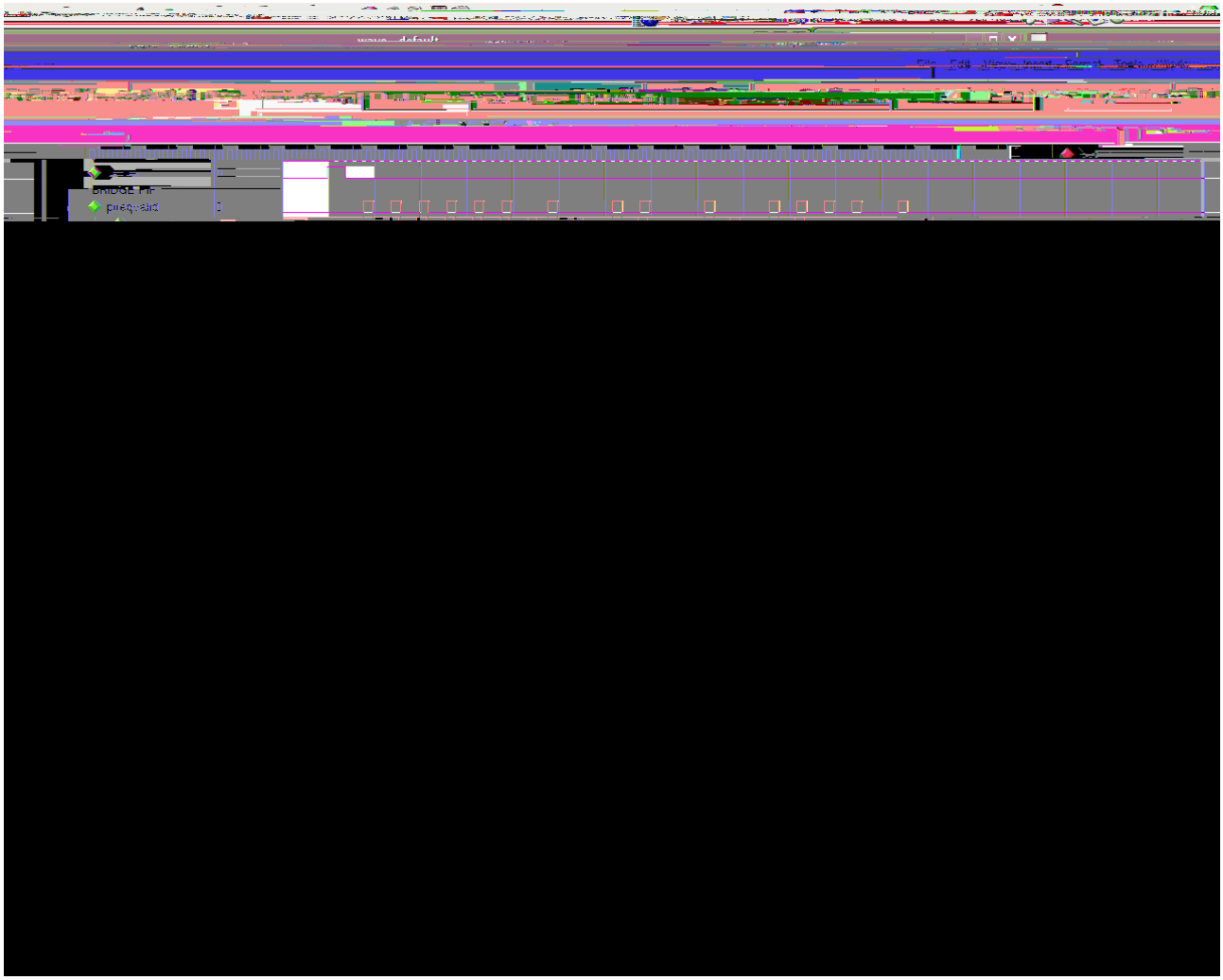


Figure 18 ± Testbench output waveform