Intel® StrongARM® SA-1100 Microprocessor

Specification Update

May 1999

Notice: The SA-1100 may contain design defects or errors known as errata. Characterized errata that may cause the SA-1100's behavior to deviate from published specifications are documented in this specification update.

Order Number: 278105-012

Contents

Revision History

Date	Version	Description
05/18/99	012	Under Documentation Changes, added changes to the PPSR and PSDR register drawing graphics; added changes to the OS Timer Interrupt Enable register; added change to the Big and Little Endian DMA Transfers graphic; corrected peripheral pin assignments; corrected SA-1100 functional diagram. Under Markings, added G stepping markings.
04/15/99	011	Documentation changes #2 - #10 have been removed from the specification update and applied to the technical reference manual; Rev G stepping information added; added doc change for big and little endian section 3.1; added documentation change for DRAM single-beat transactions Figure 10-3.
03/18/99	010	Under Documentation Changes, replaced Table 1-5; changed Section 9.5.2.1; removed section 11.12.9.3; changed current consumption units for the oscillator circuit.
02/24/99	009	Under Documentation Changes, added text change to Section 9.5.3.5; removed sentence from Section 10.6.2; changed wording in document change #1 from “all parameters guaranteed by design” to “all parameters verified by design”. Under Errata, added errata for possible PCMCIA second byte data corruption.
01/22/99	008	Under Documentation Changes, added architecture and implementation-defined identification for Register 0 of coprocessor 15; removed last sentence and changed text in the Note for Section 11.8.2; changed text in Section 10.3.2.
12/23/98	007	The document changes have been removed from the specification update and applied to the technical reference manual. The “Appendix D, Internal Test” specification change has been removed from the specification update and applied to the technical reference manual.
11/10/98	006	Under Specification Changes, added new Appendix D, Internal Test.
10/22/98	005	Under Affected Documents/Related Documents, added product discontinuance information. Under Specification Changes and Document Changes, added product discontinuance information. Under Markings, added product discontinuance information. Under Specification Changes, added product discontinuance information. Under Document Changes, added change to Table 1-1, Table 1-2, Table 8-1, and Section 11.12.4.1. Under Errata, added errata for slow SIR.
09/25/98	004	Under Affected Documents/Related Documents, added StrongARM to precede SA-1100 in the titles for the two brief datasheets.
09/18/98	003	Under Identification Information, removed DE-S1100-BA and DE-S1100-BB to show discontinuance. Under Documentation Changes, removed refererences to -BA and -BB parts to show discontinuance. On the title page, StrongARM added to precede SA-1100 in the title.

Date	Version	Description
08/25/98	002	Under Documentation Changes, changed page, table, and figure #s to show change to Intel format. Added change to Table 12-1, Table 12-2, Table 12-3, Table 13-1, Table 13-2, Figure 14-1 and Section 3.2.6. Under Identification Information, added DE-S1100-EA, DE-S1100-AB, DE-S1100-BB, DE-S1100-CB, DE-S1100-DB, AND DE-S1100-EB. Under Affected Documents/Related Documents, removed SA-1100 Data Sheet to show discontinuance. Under Errata, added two errata.
07/14/98	001	Product line order number sequence change, from 280105-001 to 278105-001. Under Affected Documents/Related Documents, changed order #s to show change to Intel order #s.
06/15/98	001	This is the new specification update document. It contains all identified errata published prior to this date.

Preface

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Intel® StrongARM® SA-1100 Microprocessor Technical Reference Manual	278088-003
Intel® StrongARM® SA-1100 Microprocessor for Portable Applications	278087-004
Intel® StrongARM® SA-1100 Microprocessor for Embedded Applications	278092-004

08/25/98
Removed reference to the StrongARM™ SA-1100 Microprocessor Datasheet (278179-001) as it is no longer in publication.

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the SA-1100 product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	E	G	#			
1	X	X		10	NoFix	Possible Missed RTC Alarm
2	X			10	Fix	Transmit Behavior Causing Generation of Five Consecutive Ones at End of CRC
3	X	X		10	NoFix	Restriction on Clearing LCD AC Bias Count (ABC) Status Bit
4	X			11	Fix	Receiver to Receive Data Frequency in Slow Infrared Mode (SIR)
5	X			11	Fix	Incorrect Transmit Pulse Width in Low-Power Mode in Slow Infrared Mode (SIR)
6	X			11	Fix	Possible Corrupted Start Bit in Slow Infrared Mode (SIR)
7	X	X		11	NoFix	Possible PCMCIA Second Byte Data Corruption

Specification Changes

No.	Steppings		Page	Status	SPECIFICATION CHANGES
	E	G			
1	X		12	Eval	USB Feature
2	X		12	Doc	Product Discontinuance

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	278088-001 278088-002 278088-003	14	Doc	AC Timing Table: Table 13-2
2	278088-001 278088-002 278088-003	14	Doc	Big and Little Endian: Section 3.1
3	278088-001 278088-002 278088-003	14	Doc	DRAM Single-Beat Transactions: Figure 10-3
4	278088-001 278088-002 278088-003	15	Doc	PPSR and PSDR Register Graphics: Section 11.13.4 and Section 11.13.6

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
5	278088-001 278088-002 278088-003	15	Doc	OS Timer Interrupt Enable Register: Section 9.4.5
6	278088-001 278088-002 278088-003	16	Doc	Big and Little Endian DMA Transfers: Figure 11-2
7	278088-001 278088-002 278088-003	16	Doc	Assignment of Signals and Serial Port Pins: Table 11-4 and Table 11-5
8	278088-003	18	Doc	SA-1100 Functional Diagram: Figure 2-2

Identification Information

Markings

This document contains errata for the SA-1100 Microprocessor. The SA-1100 device revision that is affected by this errata can be identified as order numbers DE-S1100-AA, DE-S1100-CA, DE-S1100-DA, DE-S1100-EA, DE-S1100-AB, DE-S1100-CB, DE-S1100-DB, and DE-S1100-EB for the E stepping; DE-S1100-EF and DE-S1100-EG for the G stepping.

E Stepping Markings	Speed (MHz)	Voltage (V)	Package
DE-S1100-AA	133	1.5	TQFP
DE-S1100-CA	160	2.0	TQFP
DE-S1100-DA	220	2.0	TQFP
DE-S1100-EA	190	1.5	TQFP
DE-S1100-AB	133	1.5	mBGA
DE-S1100-CB	160	2.0	mBGA
DE-S1100-DB	220	2.0	mBGA
DE-S1100-EB	190	1.5	mBGA

09/16/98
Removed markings DE-S1100-BA and DE-S1100-BB to show product discontinuance.

G Stepping Markings	Speed (MHz)	Voltage (V)	Package
DE-S1100-EF	190	1.5	TQFP
DE-S1100-EG	190	1.5	mBGA

Related Information

None for this revision of this specification update.

Errata

1. Possible Missed RTC Alarm

Problem: If an RTC alarm occurs just as the SA-1100 is entering or leaving sleep mode, the alarm status bit (AL, bit 0 in RTSR) could fail to be set.

Workaround: A software workaround intended to provide a way to avoid missing an RTC alarm is available. If the RTC alarm is set:

1. Read the RTC Timer (RCNR) and Alarm register (RTAR) before entering sleep mode via software. The RTAR must be greater than or equal to RCNR + 2 in order to ensure that an RTC alarm is not missed while entering sleep mode.
2. Read the RTC Timer (RCNR) and Alarm register (RTAR) after a sleep wakeup to determine if an alarm occurred.

Status: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

2. Transmit Behavior Causing Generation of Five Consecutive Ones at End of CRC

Problem: If the data within a packet transmitted by the SDLC transmitter causes the last five bits within the CRC to be all ones, the SDLC does not insert a zero into the serial data being output.

For example, the SDLC transmits the following:

start | addr | cntl | data | CRC...011111 | 01111110 |

when it should transmit:

start | addr | cntl | data | CRC...0111110 | 01111110 |

The SDLC receiver does not strip a zero after five ones are encountered at the end of the receive packet CRC. However, the SDLC receiver correctly detects a packet either with or without a stuffed zero at the end.

Workaround: None. Off-chip receivers can signal errors when detecting data that causes five consecutive ones to be generated at the end of the CRC.

Status: Fix. Refer to Summary Table of Changes to determine the affected stepping(s).

3. Restriction on Clearing LCD AC Bias Count (ABC) Status Bit

Problem: If the user programs the AC Bias Pin Transition Per Interrupt (API) bit-field to a nonzero value and the AC Bias Count (ABC) status bit is set, writing a one to the bit does not clear it. Only a reset of the SA-1100 can clear the ABC.

Workaround: The API should be programmed to all zeros.

Status: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

4. Receiver to Receive Data Frequency in Slow Infrared Mode (SIR)

Problem: When serial port 2 (SP2) is configured for operation in SIR mode and the remote transmitter frequency is higher by 0.13 % or more than the SP2 Sir receiver clock supplied by the 3.6864-MHz PLL and bit rate generator, some percentage of the received data is corrupted by the addition of spurious bit.

Note: According to *IrDA Serial Infrared Physical Layer Link Specification V 1.2*, the allowable rate deviation tolerance is ± 0.87% when operating in SIR mode.

Workaround: None. Off-chip IrDA receivers can be used to format and synchronize the incoming data so that it can be input to the on-chip UART via SP2.

Status: Fix. Refer to Summary Table of Changes to determine the affected stepping(s).

5. Incorrect Transmit Pulse Width in Low-Power Mode in Slow Infrared Mode (SIR)

Problem: When serial port 2 (SP2) is configured for operation in SIR mode and the UART control register 4 (UTCR4) LPB bit is set, the transmitted pulse is equal to 3/8 of a bit time.

Note: According to *IrDA Serial Infrared Physical Layer Link Specification V 1.2*, the nominal minimum pulse width is 1.63 µs regardless of the signaling rate when operating in low-power SIR mode.

Workaround: Do not use low-power (LPM) mode in SIR. Always set LPM of UTCR4 to zero.

Status: Fix. Refer to Summary Table of Changes to determine the affected stepping(s).

6. Possible Corrupted Start Bit in Slow Infrared Mode (SIR)

Problem: When serial port 2 (SP2) is configured for operation in SIR mode, there is the possibility that the loading of the Transmit FIFO while the IrDA transmitter is active can cause the transmitted start bit to be corrupted. If the problem occurs, the start bit will go active 5/16 of a bit-time too early and will remain active for 8/16 of a bit-time, instead of the required time of 3/16 of a bit-time.

Workaround: None. Off-chip IrDA transmitters can be used to format the outgoing data from the on-chip UART via SP2.

Status: Fix. Refer to Summary Table of Changes to determine the affected stepping(s).

7. Possible PCMCIA Second Byte Data Corruption

Problem: On a 16-bit data write to PCMCIA I/O space, bits [15:8] may be corrupted if the device does not assert nIOIS16, which forces two back-to-back 8-bit writes to the device. This can happen if any read/write transfers to/from addresses other than those served by the Memory and PCMCIA Control Module (that is, the Peripheral Module, the System Control Module, the LCD and DMA registers) during the PCMCIA write operation.

Implication: Unless the user controls the source code of the PCMCIA drivers allowing for a 16-bit data write to be broken into two 8-bit writes, 8-bit PCMCIA cards should not be used.

Workaround: If using an 8-bit PCMCIA device, allow only 8-bit write operations to the PCMCIA port.

Status: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

Specification Changes

1. USB Feature

The USB feature is available effective with the Rev G stepping.

2. Product Discontinuance

Effective October 16, 1998, Intel will no longer offer a 200 MHz version of the SA-1100 RISC microprocessor due to a product line consolidation. It is replaced by a new version of the same device offered at 190 MHz @ 1.5 V. This device can be ordered in both a TQFP and mBGA package.

Specification Clarifications

None for this revision of this specification update.

Documentation Changes

1. AC Timing Table: Table 13-2

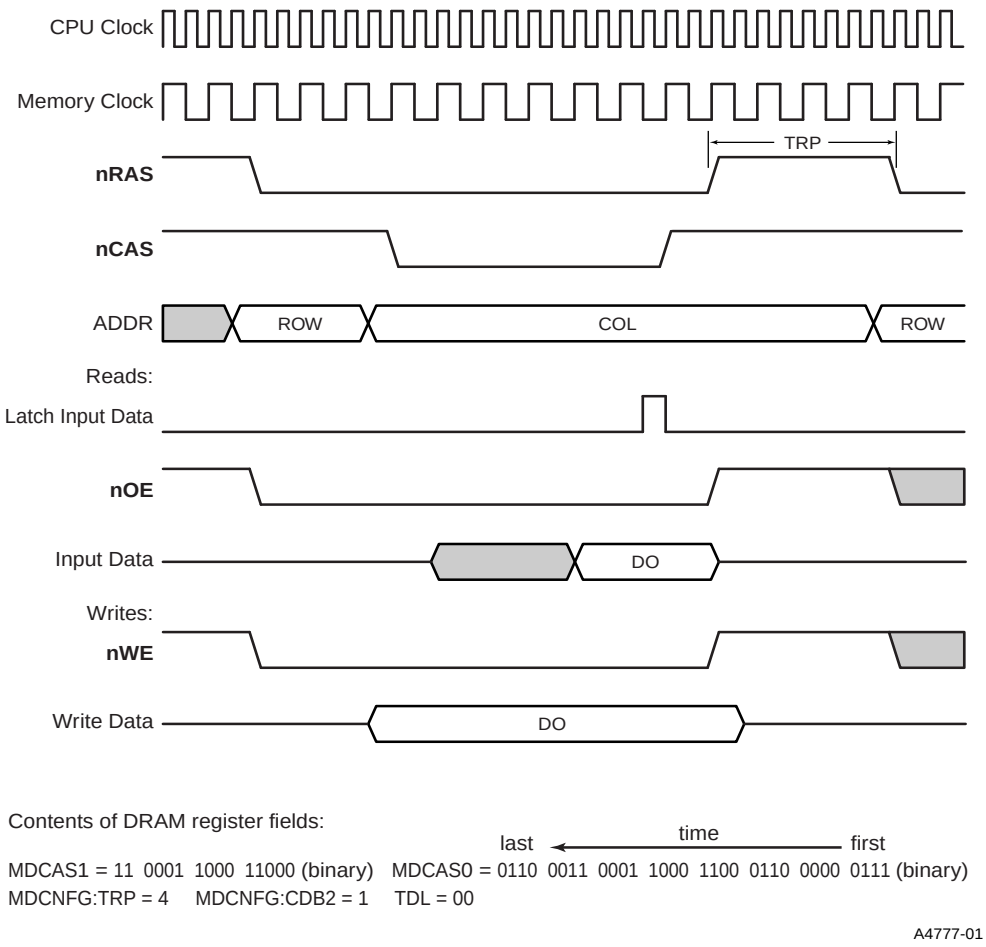
- All parameters verified by design. Data needs to be added for CA and DA parts.

2. Big and Little Endian: Section 3.1

Last sentence in fourth paragraph changed from “Instruction fetches and word load and stores are not changed by the state of the big endian bit.” to “Instruction fetches and word load and stores are not changed by the state of the big endian bit, except when those accesses are performed with memory on 16-bit data busses. See Chapter 10 for details on configuring data bus widths for various memory types.”

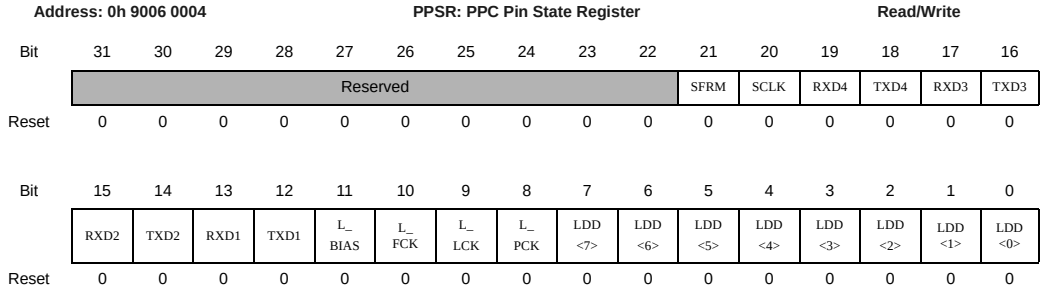
3. DRAM Single-Beat Transactions: Figure 10-3

Figure 10-3 replaced with the following figure:

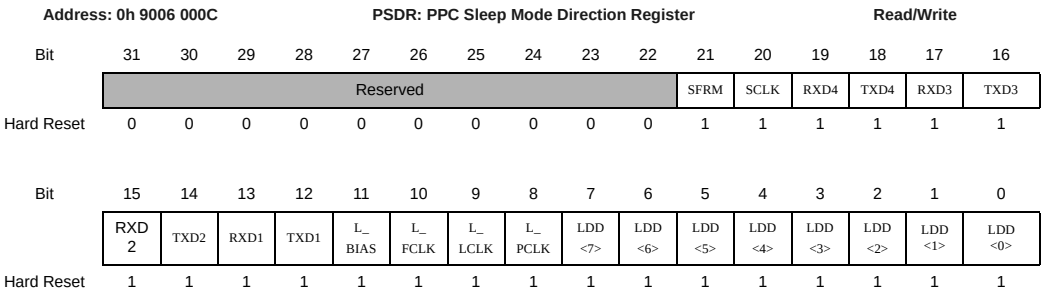


4. PPSR and PSDR Register Graphics: Section 11.13.4 and Section 11.13.6

The PPSR register graphic drawing is replaced with:



The PSDR register graphic drawing is replaced with:



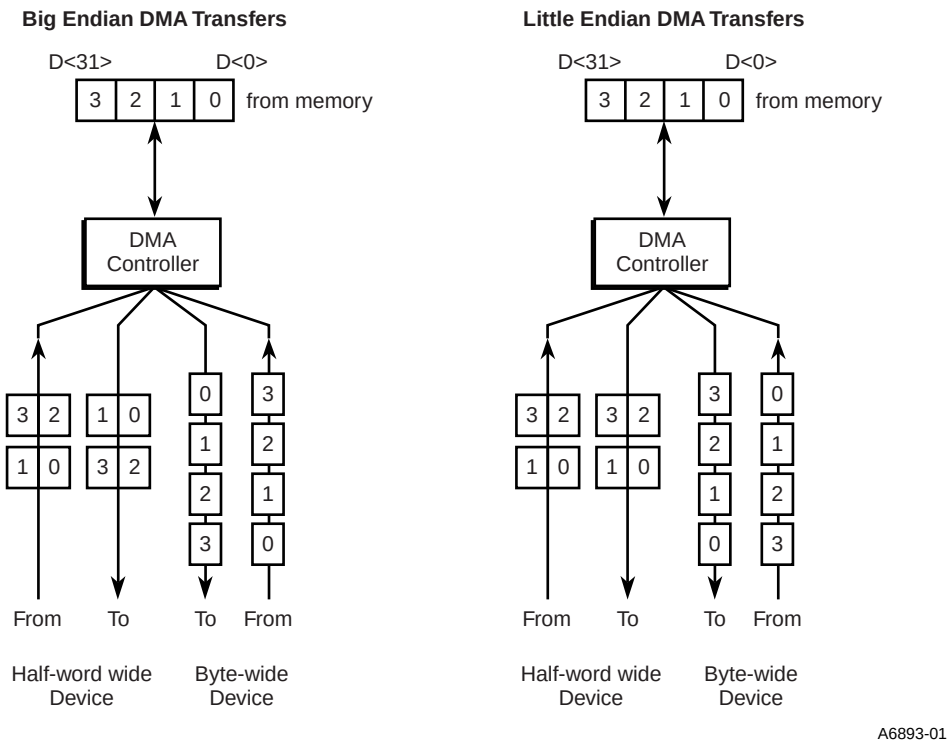
5. OS Timer Interrupt Enable Register: Section 9.4.5

The description of the OS Timer Interrupt Enable Register changed to:

Bit	Name	Description
0	E0	Interrupt enable channel 0. This bit is set by software and allows a match between match register 0 and the OS timer to assert interrupt bit M0 in the OSSR.
1	E1	Interrupt enable channel 1. This bit is set by software and allows a match between match register OSMR[1] and the OS timer to assert interrupt bit M1 in the OSSR.
2	E2	Interrupt enable channel 2. This bit is set by software and allows a match between match register OSMR[2] and the OS timer to assert interrupt bit M2 in the OSSR.
3	E3	Interrupt enable channel 3. This bit is set by software and allows a match between match register OSMR[3] and the OS timer to assert interrupt bit M3 in the OSSR.
31..4	—	Reserved.

6. Big and Little Endian DMA Transfers: Figure 11-2

Figure 11-2 replaced with:



7. Assignment of Signals and Serial Port Pins: Table 11-4 and Table 11-5

Table 11-4 “Dedicated Peripheral Pins” changed to:

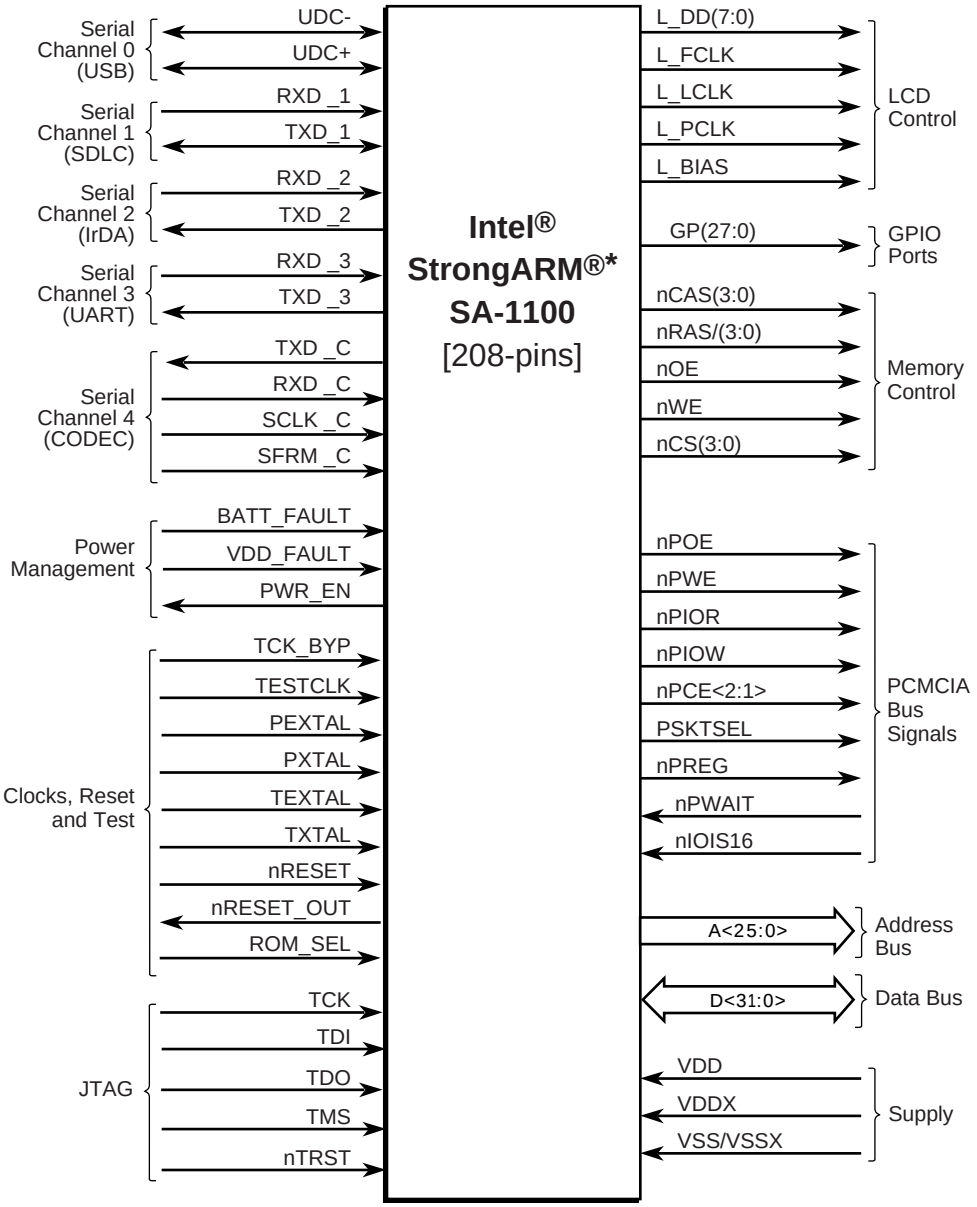
Peripheral	GPIO Pin	Function
LCD Controller	L_PCLK	Pixel clock
	L_LCLK	Line clock/horizontal sync pulse
	L_FCLK	Frame clock/vertical sync pulse
	L_BIAS	A/C bias signal
	LDD<7:0>	Pixel data
Serial port 0: USB	UDC+	Positive differential receiver
	UDC-	Negative differential receiver
Serial port 1: SDLC/UART	TXD_1	Serial transmit data
	RXD_1	Serial receive data
Serial port 2: ICP	TXD_2	Serial transmit data
	RXD_2	Serial receive data
Serial port 3: UART	TXD_3	Serial transmit data
	RXD_3	Serial receive data
Serial port 4: MPC/SSP	TXD_C	Serial transmit data
	RXD_C	Serial receive data
	SCLK_C	Serial clock
	SFRM_C	Serial frame clock

Table 11-5 “Peripheral Unit GPIO Pin Assignment” changed to:

Peripheral	GPIO Pin	Function
LCD Controller	GPIO<2>	LDD<8> pin for dual-panel color mode.
	GPIO<3>	LDD<9> pin for dual-panel color mode.
	GPIO<4>	LDD<10> pin for dual-panel color mode.
	GPIO<5>	LDD<11> pin for dual-panel color mode.
	GPIO<6>	LDD<12> pin for dual-panel color mode.
	GPIO<7>	LDD<13> pin for dual-panel color mode.
	GPIO<8>	LDD<14> pin for dual-panel color mode.
	GPIO<9>	LDD<15> pin for dual-panel color mode.
Serial port 0: USB	N/A	None.
Serial port 1: SDLC/UART	GPIO<14>	Transmit pin for UART when SDLC and UART both needed.
	GPIO<15>	Receive pin for UART when SDLC and UART both needed.
	GPIO<16>	Sample clock input/output to SDLC.
	GPIO<17>	Toggle to drive external tristate for SDLC transmit packets.
	GPIO<18>	Sample clock input to UART.
Serial port 2: ICP	N/A	None.
Serial port 3: UART	GPIO<20>	Sample clock input to UART.
Serial port 4: MPC/SSP	GPIO<10>	Transmit pin for SSP when MCP and SSP both needed.
	GPIO<11>	Receive pin for SSP when MCP and SSP both needed.
	GPIO<12>	Serial clock pin for SSP when MCP and SSP both needed.
	GPIO<13>	Serial frame clock pin for SSP when MCP and SSP both needed.
	GPIO<19>	Clock input pin for SSP to drive the frame and sample rates when other than nonmultiple of 3.6864 MHz needed.
	GPIO<21>	Clock input pin for MCP to drive the frame and sample rates when other than 12 Mbps needed.

8. SA-1100 Functional Diagram: Figure 2-2

Figure 2-2 replaced with:



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