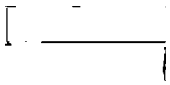


Figures

Tables

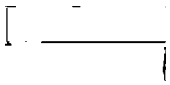


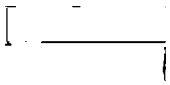
Table 2. LXT970A MII Signal Descriptions

60

Pin#[1]	Pin Name	I/O[2,3]	Signal Description[4]
			MII Data Interface Pins
63	TXD4		
62			
61			
60			
59			

			Tri-state
3	TRSTE	I	

Table 4. LXT970A Twisted-Pair Interface Signal Descriptions

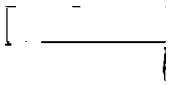


2.2.3.3 Repeater Mode

The LXT970A MII normally operates in DTE Mode (19.13 = 0). An alternative operating mode is available for repeater applications (19.13 = 1).

In Repeater Mode, the Carrier Sense (CRS) and Tri-state (TRSTE) signals request and grant bus access. The TRSTE pin controls only the receive channel of the MII (RX_DV, RX_ER, RX_CLK, and RXD).

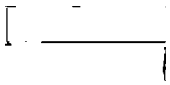
As shown in Figure 7, a central Repeater State Machine (RSM) is required to perform arbitration

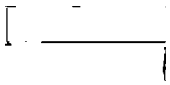


2.3.2.1 Master Clock Mode

The Master Clock mode is recommended in most Network Interface Cards (NICs) and switch

2.3.3 Bias Circuit Requirements





2.8.1.4 Collision Indication

Figure 18

2.8.1.5 SQE (10T Only)

When the SQE (heartbeat) function is enabled, the LXT970A asserts its COL output for 5-15 BT after each packet. By default, the SQE function is disabled on the LXT970A. To enable SQE, set bit 19.10 = 1. See Figure 30 on page 59 for SQE timing parameters.

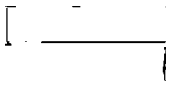
2.8.1.6 Jabber (10T Only)

If the MAC transmission exceeds the jabber timer, the LXT970A disables the transmit and loopback functions and asserts the COL pin. The LXT970A automatically exits jabber mode after 250-750 ms. This function can be disabled by setting bit 19.9 = 1. See Figure 31 on page 59 for Wrt6.3(e)1(PM Tw[aye51 1sWWrt6.[(W)51k[(2).1(a[(W)51d0.8r(1s)-5ri7r srn)-5trt6.utran.6())]T3(e)1fu[(W)51cabber.1

3.0 Application Information

3.1 Magnetics Information

3.2 Crysal78.2(ll78.2nm)-4.6(f-10.5(o)-4.6ro)625()873.5(a)2.2ion



3.3.5.2 Fiber

The fiber interface consists of a pseudo-ECL transmit and receive pair to an external fiber optic transceiver. The transmit pair should be AC-coupled to the transceiver, and biased to 3.7V with a 50Ω equivalent impedance. The receive pair can be DC-coupled, and should be biased to 3.0V with a 50Ω equivalent impedance.

Figure 22. MII - 100BASE-TX Receive Timing / 4B Mode

Figure 24. MII - 100BASE-TX Receive Timing / 5B Mode

Figure 27. MII - 100BASE-FX Transmit Timing / 4B Mode

Table 36. MII - 100BASE-FX Transmit Timing Parameters / 4B Mode

Parameter	Sym	Min	Typ[1]	Max	Units[2]
TXD<3:0>, TX_EN, TX_ER Setup to TX_CLK High	t6A	10	–	–	ns

Figure 29. MII - 10BASE-T Transmit Timing

Table 38. MII - 10BASE-T Transmit Timing Parameters

Figure 30. 10BASE-T SQE (Heartbeat) Timing

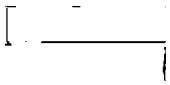
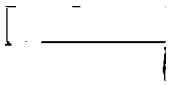


Figure 34. MDIO Timing when Sourced by STA

Figure 35. MDIO Timing when Sourced by PHY

Table 42. MDIO Timing Parameters



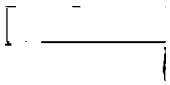
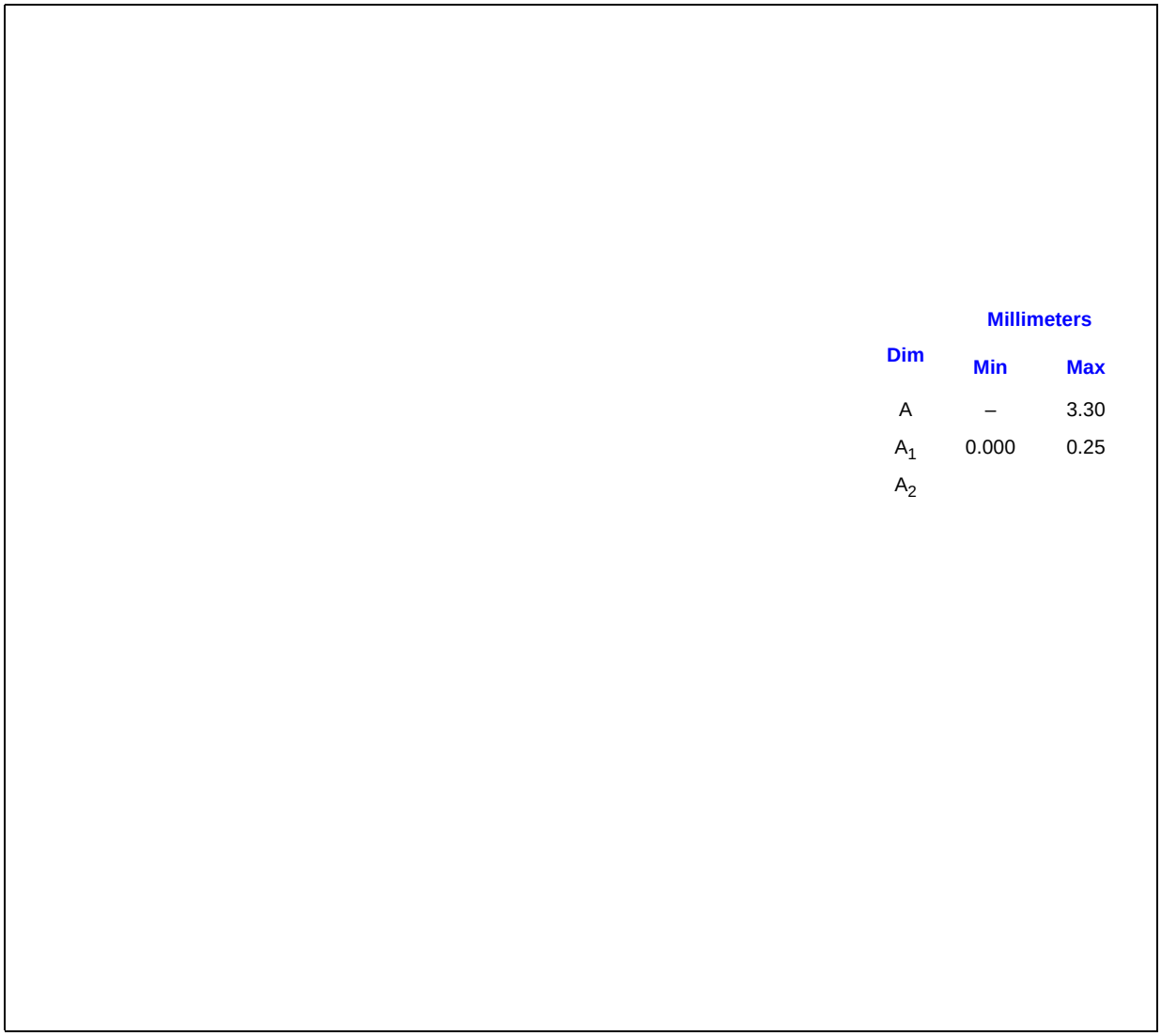


Table 51. Auto Negotiation Expansion (Address 6)

19.2	100BASE-FX	1 = Enable 100BASE fiber interface.

6.0 Mechanical Specifications

Figure 38. 64-Pin QFP Package Diagram



Dim	Millimeters	
	Min	Max
A	–	3.30
A_1	0.000	0.25
A_2		