I2C-Master Core Specification

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Revision History

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Registers

3.1 Registers list

Name Address Width Access Description

3.2.6 Status register

Bit #	Access	Description
7	R	RxACK, Received acknowledge from slave. This flag represents the addressed slave's acknowledge. '1' = No acknowledge received '0' = Acknowledge received
6	R	Busy, I2C bus busy '1' after START signal detected '0' after STOP signal detected
5:2	R	*Reserved*
1	R	TIP, Transfer in progress. '1' when transferring data '0' when transfer complete

Example 2

Read a byte of data from an I2C memory device.

Slave address = 0x4E
Memory location to read from = 0x20

I2C sequence:
1) genera11.2E